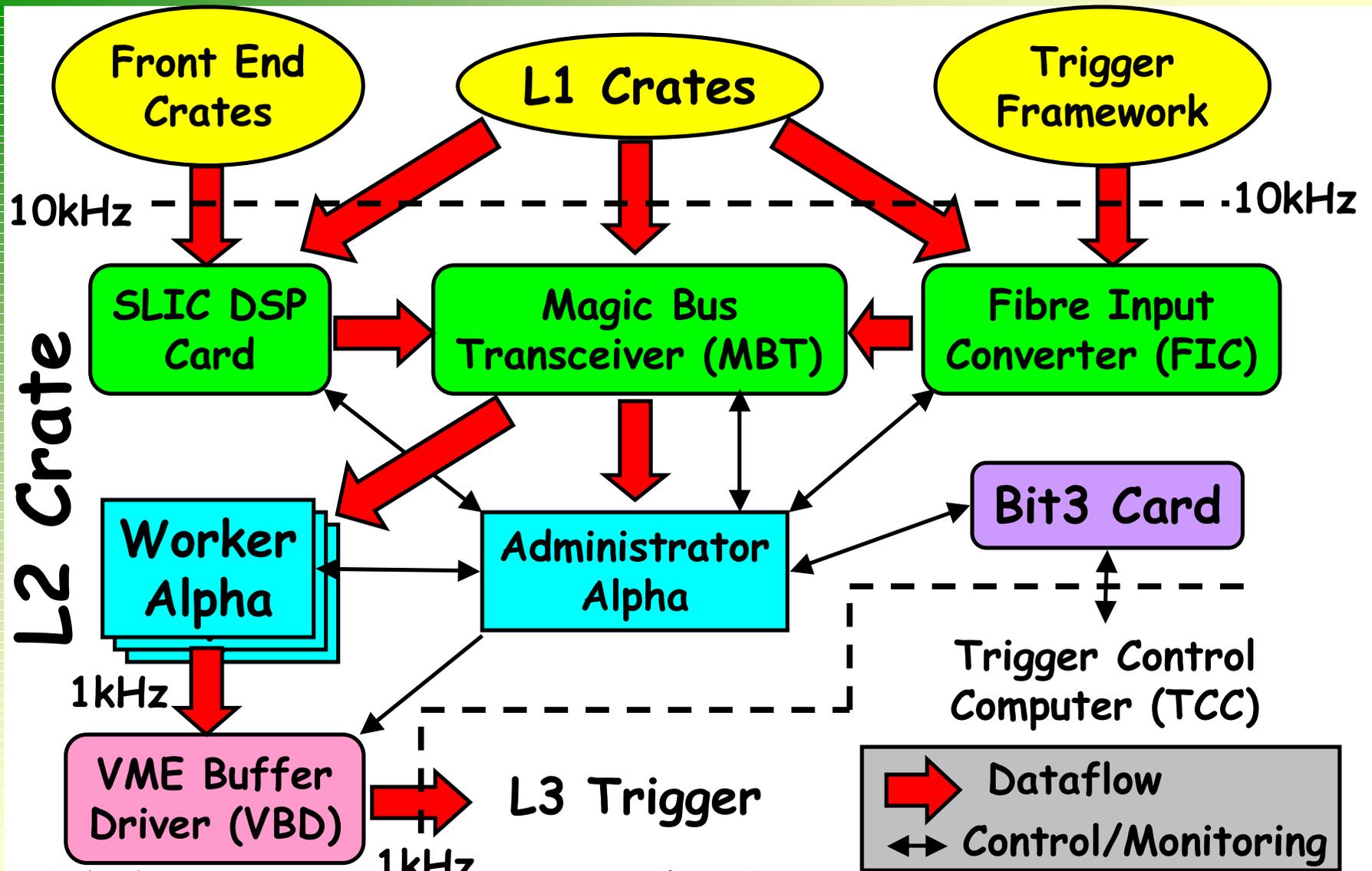


Status of the L2 Trigger

Roger Moore
Michigan State University

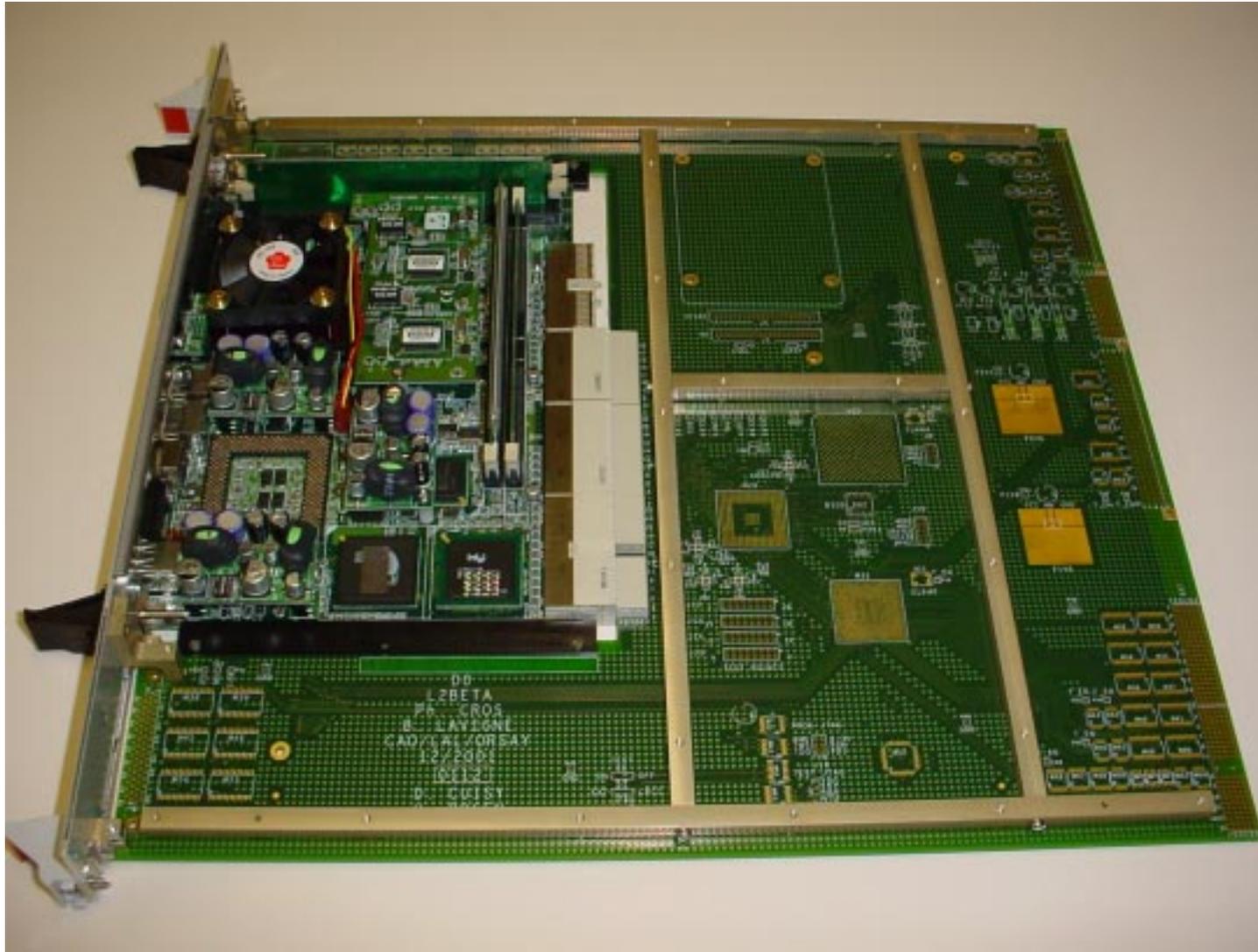
L2 System Overview



Hardware Status

- **MBT: monitor data readout being tested**
 - Multi-MBT firmware problem fixed
- **SLIC: need firmware fix to write out inputs**
- **SFO (fans out serial inputs to MBT/SLIC)**
 - Enough for full L2 system w/o SLIC shadowing
- **13 Alpha Processor Boards working reliably**
 - Enough for single Alpha system + a little beyond
- **First Beta prototype arrives this week**
 - Testing this month, 2nd prototype ~2 weeks later
 - Plan for production over summer, install autumn
- **Silicon Tracking Trigger (STT)**
 - Arrives ~July

Level 2 β Prototype



20/02/2002

R. Moore, Michigan State

4

Remaining Hardware Issues

- **Magic Bus arbitration (Rick Kwarciany)**
 - Original scheme from UMich used PECL arbitration scheme: too much noise
 - MBT and Alpha now converted to new TTL arbitration scheme
 - Successfully tested at the L2 test stand
- ...however with successful arbitration new Alpha PIO FPGA bugs were found
 - Fixes in progress...also affects CDF
- Limited to single Alpha and lock-step event loop until these problems are fixed

Software Status

- State machine architecture
 - Each state performs single action
 - Setup DMA, read L2 decision, start L3 readout etc.
 - Allows extreme flexibility to handle varying hardware configurations
 - Configured by L2 parser
 - Reduces L2 to a single executable
 - Makes versioning a lot easier
- Basic structure well tested and stable
 - Running in L2mu, L2cal and L2global crates
 - One remaining synchronization problem between data buffer and L2 decision after SCL INIT is being worked on
 - Have to fix before rejection

Monitoring

- **Software Monitoring**
 - Data path (Alpha→TCC→display) tested
 - Online code has a collect status state and generates data
 - Currently working on display
- **Hardware scaler monitoring**
 - Provide information even if the Alpha crashes
 - Cables laid for F+C muon PP crates
 - State scalers implemented
 - Buffer occupancy scalers next
 - Not very useful before non-lockstep event loop mode

L2 Configuration

- L2 configured using built in parser
 - No RCPs online
- Current scheme uses hand written config files stored on disk
 - Can use COORsim to generate Global configuration from database
- Final scheme uses COOR→TCC→Alpha data path with two phase configuration
 - Phase 1: hand written hardware configuration
 - e.g. cards' VME slots - not relevant to Physics
 - Phase 2: COOR commands buffered by TCC for Alpha download
 - See <http://www-clued0.fnal.gov/~rwmooore/l2config.html>

Available Inputs

- **Muon**
 - All types are available (few dead channels)
 - Front-end inputs being decoded correctly
 - Now working on decoding L1 inputs
- **Calorimeter has inputs for $|\eta| < 0.8$**
 - No L2 header (with tick/turn) or seed mask
 - Varying pedestals in η ($\sim 1\text{GeV}$)
 - Gain not normalized to precision readout
 - Need 0.5 GeV steps for E_{TOT} not 0.25 GeV
 - **Currently using software patch**
 - **Compromises performance**
- **Remaining inputs:**
 - **CPS in March?** - **CTT in April?**
 - **FPS in May?** - **STT in July?**

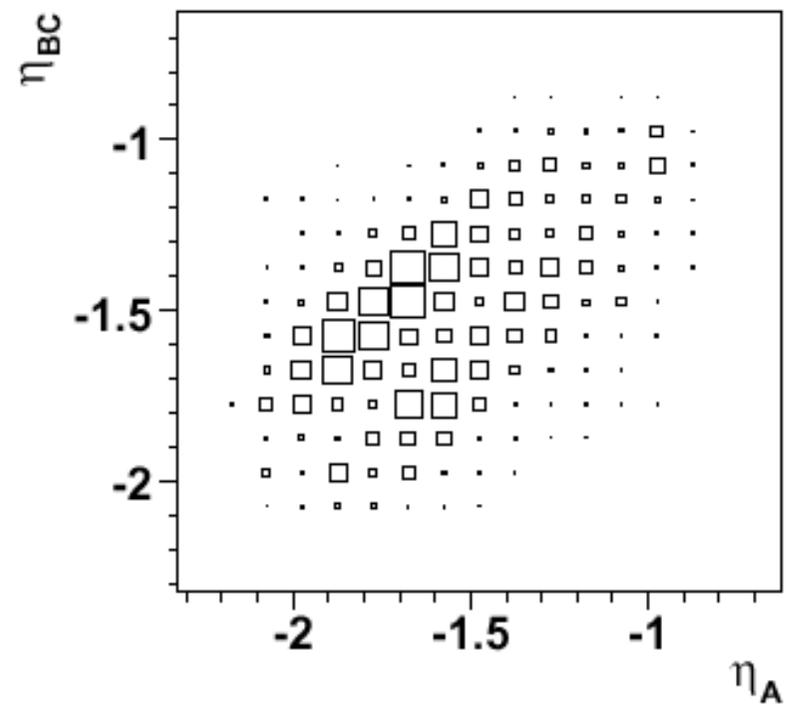
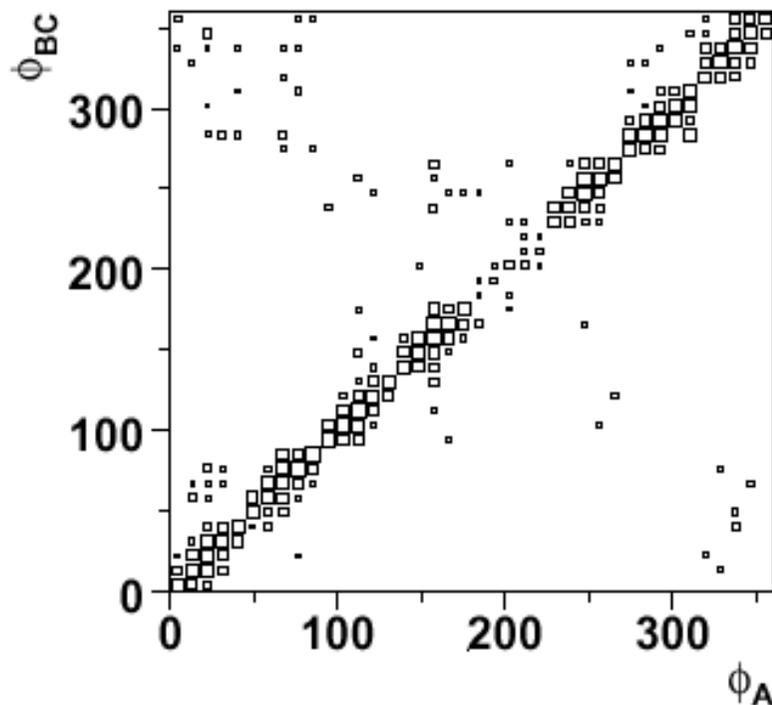
Currently Running Crates

- Both L2 Muon Pre-processors (F+C)
 - Running since October shutdown with limited inputs
 - All SLICs present and running
 - Track finding algorithm now being tuned
- Calorimeter (EM+Jets)
 - Running since December
 - 3x3 jet algorithm
 - First combined EM+Jets worker exists
 - Outputs both algorithms' data to L3
 - Working on sending both to L2 global (now just EM)
 - Difficult because original design had separate workers

L2 Muon Pre-Processor

A \leftrightarrow BC Matching (all combinations)

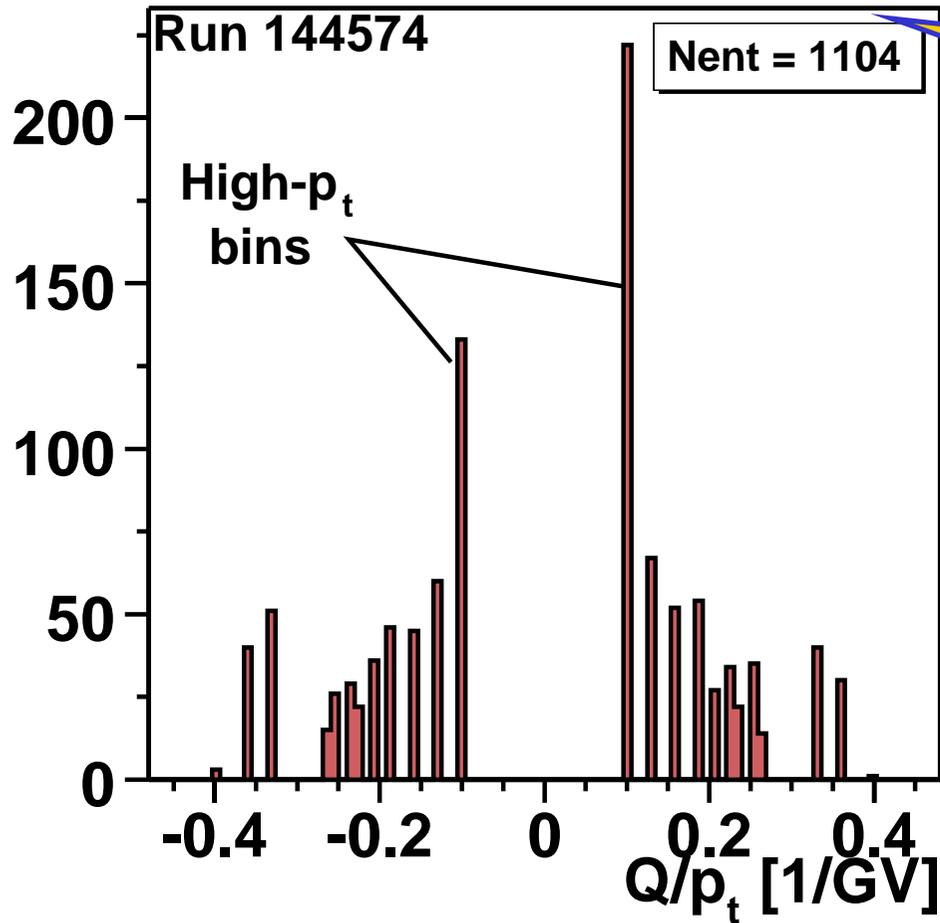
13th December Global Run, 150k Events



Log-scale for boxes to emphasize single events

L2 Muon P_T Measurement

P_t Measurement in Central L2- μ

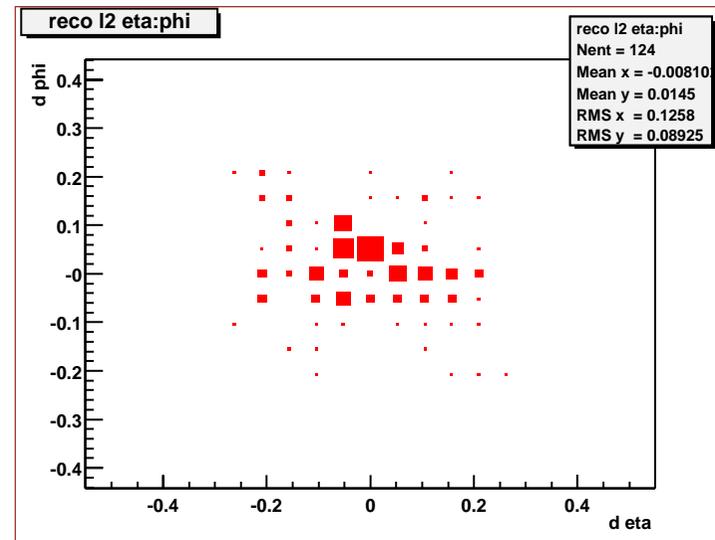
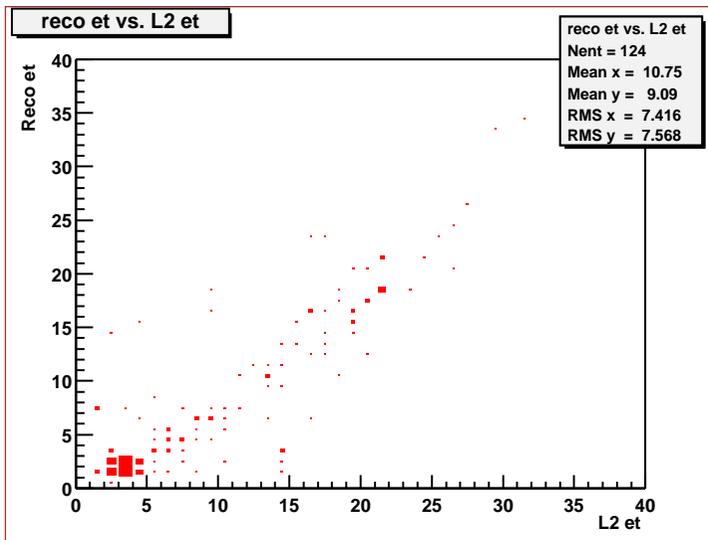
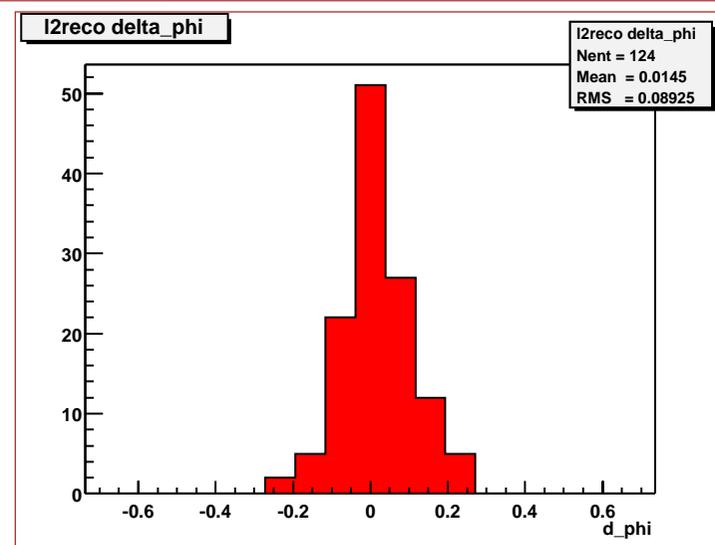
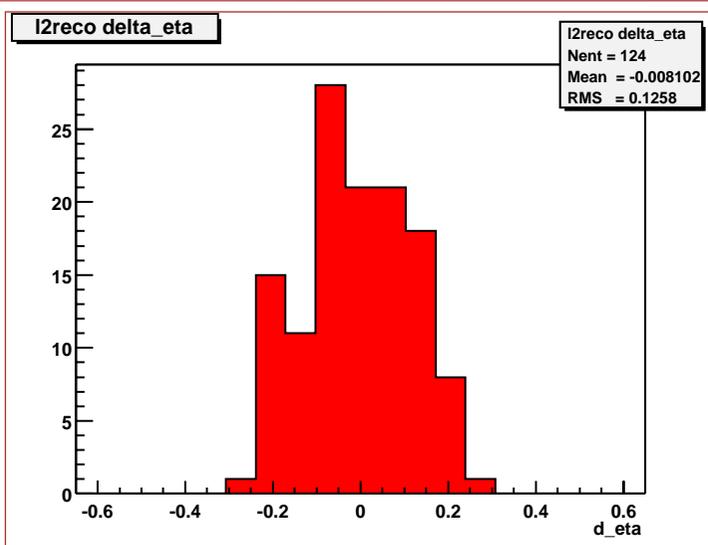


First Look!

Trigger
Simulator
Running on
Real data

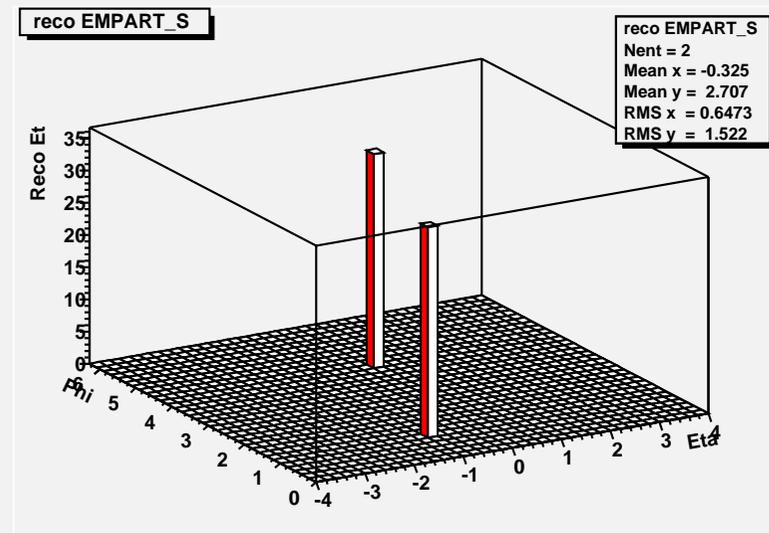
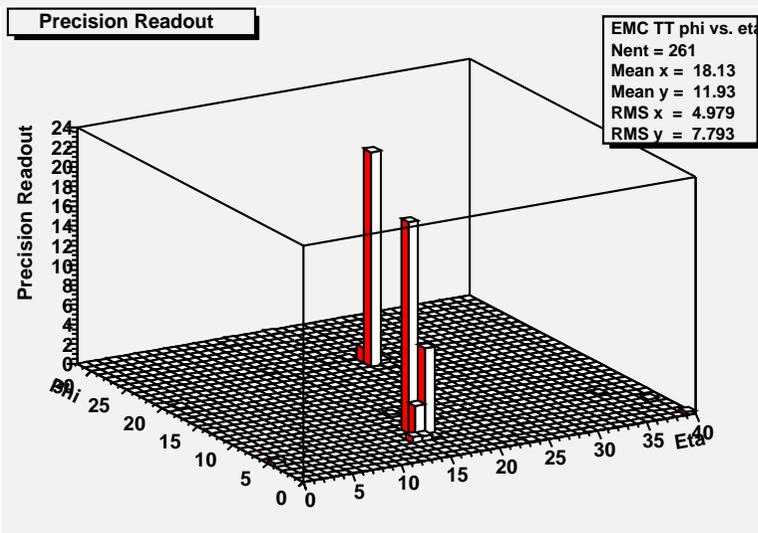
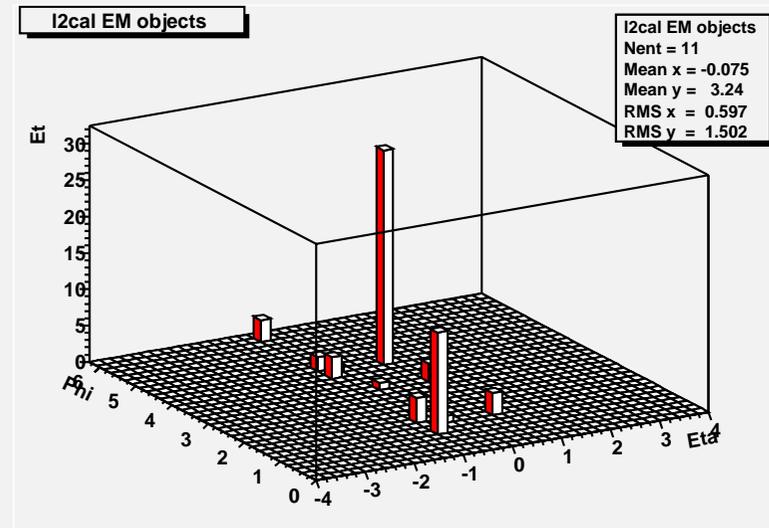
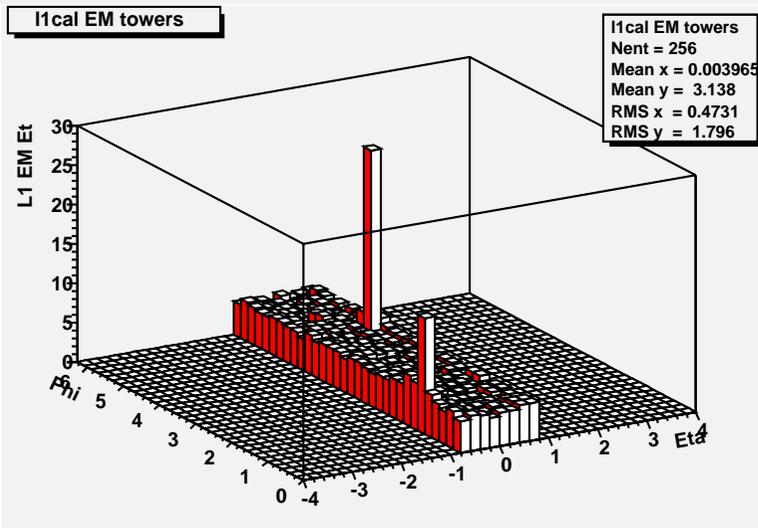
L2 Cal EM Pre-processor

Run 144060, Events 1-500

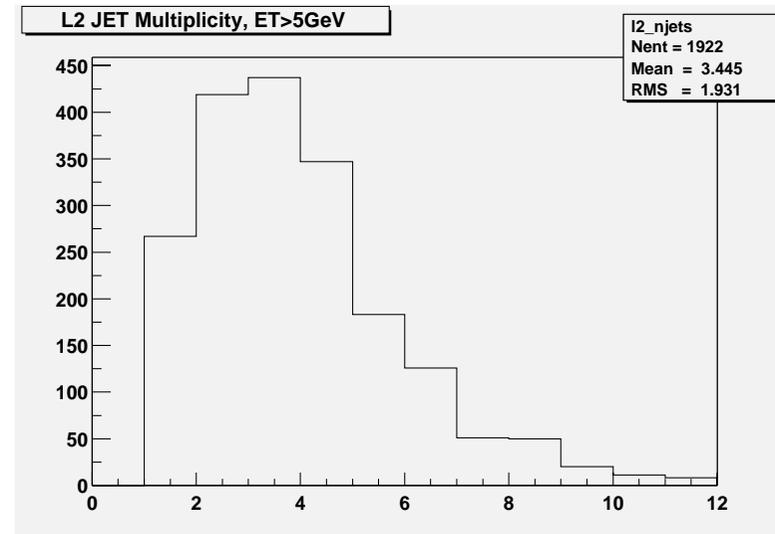
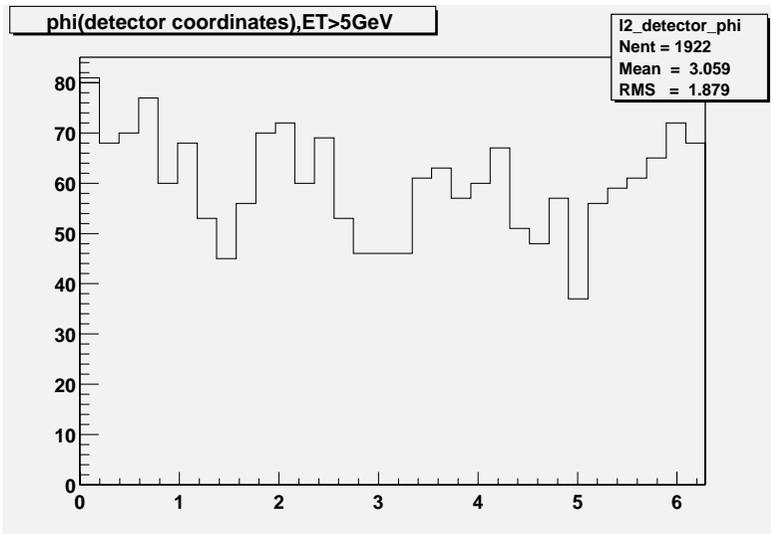
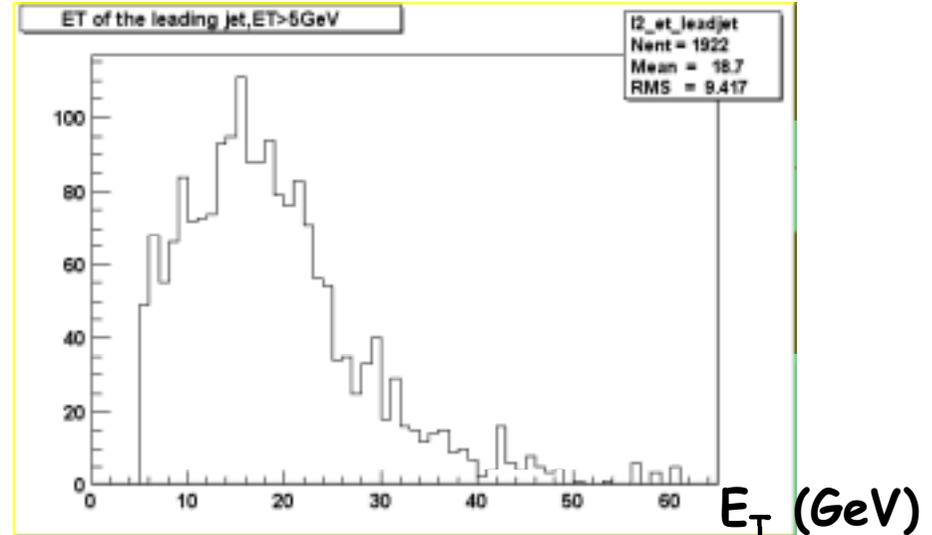
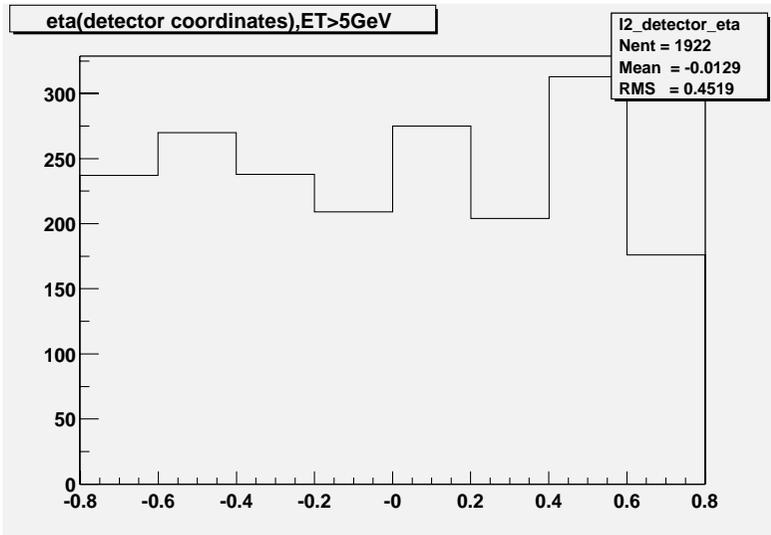


"Typical" Event Comparison

Run 144060, Event 467



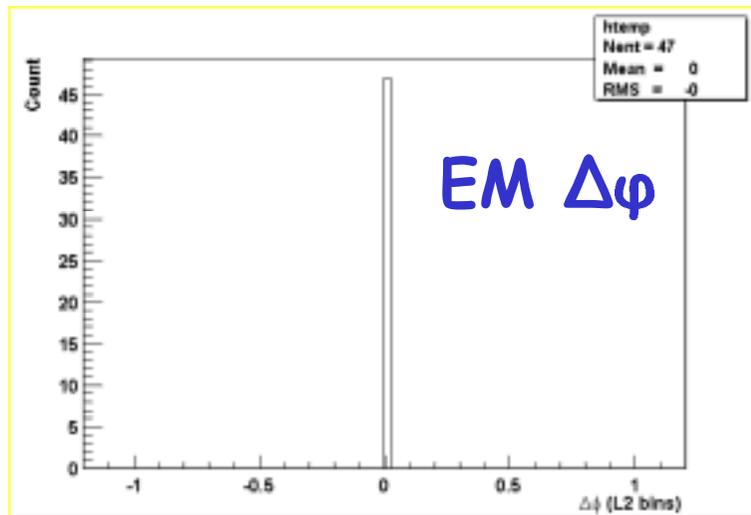
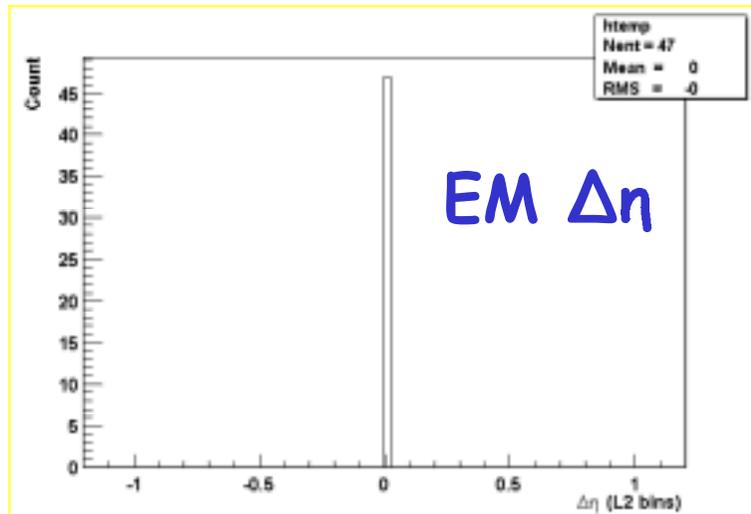
L2 Cal Jet Pre-Processor



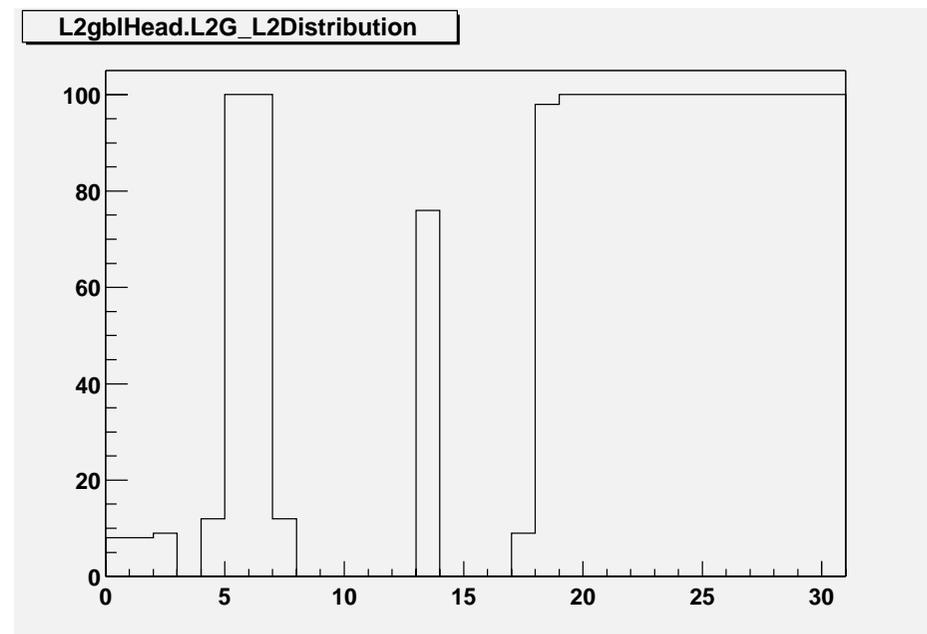
L2 Global Crate

- Now running online with Cal and Muon PP inputs
- Running without L1 trigger bits
 - Decoding works fine but...
 - Including these prevents multiple, concurrent runs in DAQ
 - trigger framework sends bits sent for ALL triggers
- All scripts run every event
 - 5 test scripts configured
 - Observed to pass and fail
 - Physics objects consistent with input data
 - No tracking input yet so no matching possible

L2 Global Processor



Example script pass fractions
for Monte-Carlo



L2 TrigSim

- Latest test release (t02.05.00) contains working L2 TrigSim
 - I/Ogen byte swapping issues finally(?) laid to rest...not a simple task
 - File→DSPACK→CPU order→data order
 - ...plus some data stored inside VRB!
 - Rapid online code changes slowed/stopped
 - Improves offline stability
- Now run analyse packages on raw and MC data
 - Calorimeter tested, muon being tested
 - Almost ready for rate and efficiency studies

Before Rejection...

- Technically readiness
 - Test writing L2 bits to framework (<1week)
 - Fix SCL_INIT synchronization bug
- Must run online software from online release i.e. l2onlxx.xx.xx (~1 week)
 - Required for reproducibility later
 - Currently ~1 bug fix away from this
 - Base this release on a 'p' release
 - Currently use 't' releases as base
- Offline use production release
 - Stable base for algorithm tuning
 - Needed to use MC farms
 - Generate root-tuples for non-expert use
 - Plan to use re-release of p11 in 2-3 weeks time

Before Rejection...

- Would like to have COOR download too
 - Difficult to reconfigure L2 "on the fly" w/o it
- Measure rejection and efficiency
 - Demonstrate improvement over pre-scaling
 - i.e. $\text{efficiency} > 1/\text{rejection}$
- Measure throughput and latency
 - Current max rate estimate is ~2kHz
 - Single Alpha+Linux in Cal crate with L1Cal seed mask
 - Readout not yet buffered
 - So L2 latency = dead time
- Stable (not rapidly changing) code
 - Low rate of releases

Status Summary

- Hardware sufficient for ~2kHz rate
- Software framework in place and running
 - Script download only big missing feature
- One test and one bug-fix away from "technical readiness" milestone
 - Send L2 bits to trigger framework
 - Done next week...if so ahead of schedule
- Remaining pre-processors (CPS,FPS,CTT)
 - Online ~4-8 weeks after inputs available
- L2STT online late summer

Conclusion

- Now entering the verification/certification phase
 - Need input from TCB/Collaboration on how much is required before rejection
- Help needed from
 - ID groups to measure efficiency vs. L1/L3/Reco
 - Physics groups to measure efficiency/rejection for different MC signals
 - Common object comparison interface
 - Talk to Reiner Hauser <rhauser@fnal.gov>
- Expect the L2 trigger to start rejecting in ~4-6 weeks
 - ...subject to TCB/Collaboration feedback